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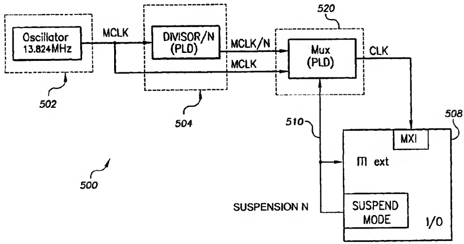
(54) Title: REDUCTION OF POWER CONSUMPTION WITH INCREASED STANDBY TIME IN WIRELESS COMMUNICATIONS DEVICE



(57) Abstract: A method and apparatus for reducing power consumption of a receiver of a communications device that does not change the global hardware of the device and uses the current master clock to lower the clock frequency. In an example embodiment, a method directed to reducing power consumption of a receiver of a communications device during an idle state. The receiver has an internal power source and a corresponding base unit. The method includes generating a clock signal that has an output frequency that varies, the frequency being higher in an active state and lower in an inactive state, such that the receiver consumes more power during the active state than when in the inactive state. Power consumption by the receiver is reduced by dynamically and synchronously switching the clock frequency to a lower clock frequency. Receiver power consumption is a function of the power consumed during the active and inactive states and the duration of the idle state.

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REDUCTION OF POWER CONSUMPTION WITH INCREASED STANDBY TIME IN WIRELESS COMMUNICATIONS DEVICE

Field of the Invention

This invention generally relates to a power conserving arrangement for, and method of, minimizing battery power consumption during stand-by operation of a portable, battery-operated, mobile device and, more particularly, a wireless telephone system.

Background of the Invention

A typical cellular telephone communicates with a base station, the base station transmitting messages to the cellular telephone on a regular basis. Similarly, a cordless telephone communicates with the base unit and remains ready to respond to any incoming call. These telephones usually include some form of a transceiver and a decoder under microprocessor control.

During a standby mode of operation, the telephone waits to receive a telephone call through the base unit. During the stand-by mode of operation, the telephone continuously receives and decodes all messages transmitted by the base unit and synchronizes itself with the base unit regularly. The telephone consumes electrical power in both the talk and the standby modes. In cordless battery-operated telephones, the on-board battery typically has a working lifetime of approximately 100 hours in the stand-by mode and about 10 hours in the talk mode (in the DECT standard as an example). The battery is then re-charged or replaced to continue telephone service. The microprocessor and other electronic components onboard the telephone are energized during the standby mode which contributes to current drain on the battery. The need to increase the battery lifetime between re-charges and/or battery replacement is self-evident.

Cordless telephones, while in an idle or standby mode, constantly monitor a continuous stream of signals sent by the base unit. Typically, the cordless telephone uses a dotting sequence, the first segment of the message to synchronize the telephone hardware to a master clock frequency in the base. The portable unit or handset

(cordless or cellular) needs to be synchronized with the base station and transmitted signal to allow for accurate and reliable communication.

In order to preserve power of the battery in the handset, the receiver portion or the handset moves into an idle locked mode or standby mode waiting for an actual call to come in. The handset typically powers down during the standby mode but the internal communication circuits need to remain in synchronization with the base station signal, thereby consuming battery power. It would be commercially advantageous to provide a method and an apparatus for reducing power consumption during the standby mode without increasing cost or hardware complexity.

Summary of the Invention

The present invention is exemplified in a number of implementations and applications, some of which are summarized below. One of the advantages of the present invention is the ease of incorporation of the method into existing wireless telephones without significant hardware or software redesign. Accordingly, a method is described herein that addresses this need of reducing power consumed by a receiver of a communications device. In an example embodiment, the receiver has an internal power source and a corresponding base unit. The receiver of the communications device is adapted to receive a transmitted signal in the form of a data stream, the data stream defined by a plurality of frames, each of the frames including a synchronization sub-frame. The method includes detecting the activity status of the receiver with respect to the transmitted signal, the receiver being in an idle state when not receiving a transmitted signal. The idle state is defined by a predetermined number of frames that include a set of active state frames and inactive state frames that combine to defined a duration of the idle state. A clock signal is generated that has an output frequency that varies as a function of the active and inactive frames. The clock frequency is higher in the active state and lower in the inactive state, such that the receiver consumes more power during the active state then when in the inactive state. The receiver is then synchronized with the sub-frame of the transmitted signal during the idle state. Power consumed by the receiver is then reduced by reducing the clock frequency as the number of inactive frames within the idle state are

increased. In the present invention, the power consumed by the receiver is a function of the power consumed during the active and inactive states and the duration of the idle state.

According to another aspect of the invention, a method is directed to reducing power consumption of a receiver of a communications device during an idle state mode. The receiver has an internal power source and a corresponding base unit. The receiver of the communications device is adapted to receive a transmitted signal in the form of a data stream defined by a plurality of frames. The idle state is defined by a predetermined number of frames that include a set of active state frames and inactive state frames that combined to define a duration of the idle state. The method includes generating a clock signal that has an output frequency that varies as a function of the active and inactive frames. The clock frequency is higher in the active state and lower in the inactive state, such that the receiver consumes more power during the active state then when in the inactive state. The receiver is then synchronized with the sub-frame of the transmitted signal during the idle state. The power consumed by the receiver is then reduced by dynamically and synchronously switching the clock frequency to a lower clock frequency. The lower clock frequency corresponds to the inactive state and the increased number of inactive frames within the idle state. The power consumed by the receiver is a function of the power consumed during the active and inactive states and the duration of the idle state.

In yet another aspect of the invention, a system for reducing power consumption of a receiver of a communications device is described. The receiver has an internal power source and a corresponding base unit. The receiver is adapted to receive a transmitted signal in the form of a data stream, the data stream defined by a plurality of frames, each of the frames including a synchronization sub-frame. The system includes a detector adapted to detect the activity status of the receiver with respect to the transmitted signal. The receiver is in an idle state when not receiving a transmitted signal, the idle state defined by a predetermined number of frames that include a set of active state frames and inactive state frames that combined define a duration of the idle state. A clock signal generator coupled to the detector generates a clock signal with an output frequency that varies as a function of the active and

inactive frames. The clock frequency is higher in the active state and lower in the inactive state, such that the receiver consumes more power during the active state then when in the inactive state. Synchronizing circuitry, coupled to the receiver and the clock signal generator, synchronizes the receiver with the sub-frame of the transmitted signal during the idle state and reduces the power consumed by the receiver. The power consumed by the receiver is reduced by reducing the clock frequency by increasing the number of inactive frames within the idle state. The power consumed by the receiver is a function of the power consumed during the active and inactive states and the duration of the idle state.

In yet another aspect of the invention, an apparatus is directed to reducing power consumption of a receiver of a communications device during an idle state. The receiver has an internal power source and a corresponding base unit. The receiver is adapted to receive a transmitted signal in the form of a data stream defined by a plurality of frames. The idle state is defined by a predetermined number of frames that include a set of active state frames and inactive state frames that combine to define a duration of the idle state. The apparatus includes a clock signal generator that has an output frequency that varies as a function of the active and inactive frames. The clock frequency is higher in the active state and lower in the inactive state, such that the receiver consumes more power during the active state then when in the inactive state. The apparatus further includes circuitry for synchronizing the receiver with the transmitted signal during the idle state, the circuitry coupled to the receiver and the clock signal generator. The apparatus also includes a mechanism adapted to reduce the power consumed by the receiver that is coupled to the clock generator. The mechanism dynamically and synchronously switches the clock frequency to a lower clock frequency corresponding to the inactive state that has an increased number of inactive frames within the idle state. The power consumed by the receiver is a function of the power consumed during the active and inactive states and the duration of the idle state.

The above summary is not intended to provide an overview of all aspects of the present invention. Other aspects of the present invention are exemplified and described in connection with the detailed description.

Detailed Description of the Drawings

Various aspects of, discoveries made in connection with, and advantages of, the present invention will become apparent upon reading the following detailed description of various example embodiments and upon reference to the drawings in which:

FIG. 1 is a schematic of an example prior art communication system between a base station or unit and a handset or receiver;

FIG. 2 is a timing diagram of the master clock during the idle or suspend mode, resulting from an example embodiment of the present invention;

FIG. 3 is a timing diagram illustrating levels of power consumption during active and inactive states of the suspend mode, resulting from an example embodiment of the present invention;

FIG. 4 is a schematic of the master clock signal generator coupled to the global logic of the receiver, representing an example embodiment of the present invention;

FIG. 5 is a global schematic of the master clock signal generator coupled to other components of the receiver, representing an example embodiment of the present invention;

FIG. 6 is a timing diagram illustrating an example of the suspend signal switching off the power to the receiver, made in accordance with an example embodiment of the present invention; and

FIG. 7 is a schematic of the global logic implementing the example embodiment described in FIG. 6, made in accordance with an example embodiment of the present invention.

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention to any particular embodiment described. On the contrary, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

Detailed Description of the Invention

The present invention may be applied to a variety of wireless communication systems and devices, the power reduction method and system has been found to be advantageous for use in connection with cordless telephones and portable wireless devices needing to conserve battery power. While the present invention is not necessarily so limited, an appreciation of various aspects of the invention may be obtained through a discussion of various application examples.

In one example application of the present invention, a method for reducing power consumption of a receiver of a communications device during an idle state mode is described. The receiver has an internal power source and a corresponding base unit. The receiver of the communications device is adapted to receive a transmitted signal in the form of a data stream defined by a plurality of frames. The idle state mode has a predetermined number of frames that include a set of active state frames and inactive state frames that combined to define a duration of the idle state. The method includes generating a clock signal that has an output frequency that varies as a function of the active and inactive frames. The clock frequency is higher in the active state and lower in the inactive state, such that the receiver consumes more power during the active state then when in the inactive state. The receiver is then synchronized with the transmitted signal during the idle state. Overall power consumption by the receiver is then reduced by dynamically and synchronously switching the clock frequency to a lower clock frequency. The lower clock frequency corresponds to the inactive state and the increased number of inactive frames within the idle state. Overall power consumption is a function of the power consumed during the active and inactive states and the duration of the idle state.

In another example application, a cordless telephone would have circuitry incorporated in the handset that would be synchronized with the base unit for reducing power consumption by the handset when no communications is actively occurring. The clock frequency within the handset can be reduced without the use of a second crystal oscillator that would clock at a lower frequency to conserve power. The current master clock frequency can be switched dynamically and synchronously to a

lower frequency by dividing the clock signal by a predetermined divisor, via divisor circuitry. The handset is readied for resynchronization with the base unit by an internal timing signal to avoid prolonged periods of inactivity leading to the handset loosing synchronization due to "too much sleep".

Referring now to FIG. 1, a schematic 100 of an example prior art wireless communications system between a base station or unit and a handset or receiver is illustrated. The communications system 100 includes a fixed part 102, with an antenna 103 for transmitting a signal 106, and a portable part 104, with an antenna 105 for receiving the transmitted signal 106. Although not shown, in many applications both parts have receiving and transmitting arrangements. The fixed part can be, for example, a base station transmitter for cellular communications or a base unit for wireless communication at home. The portable part can be a cellular telephone or a portable handset for residential use. This example can also represent wireless communication with wireless portable devices such as PDAs (personal digital assistants) or paging devices or PCs with wireless modems. With respect to the present invention, system 100 represents a cordless telephone system, but the teachings of the present invention are not limited to this example embodiment. As shown, the communications standard that applies in the system can be either the European DECT standard or the North American PWT for transmitting and receiving signals in the form of frames composed of bits.

In normal operation, portable part or receiver 104 is synchronized with the signals that are being transmitted regularly from fixed part or base unit 102. Receiver 104 enters into a standby or idle locked mode when regular communications are not detected in order to conserve battery power. However, at all times receiver 104 remains in synchronization with base unit 102 to ensure accurate and reliable communications. Between synchronization cycles, receiver 104 activity is very low and it does not require the same clock frequency than when in an active mode. During this power down or standby period some systems go into a sleep mode to conserve energy, but there is a concern that receiver 104 will lose synchronization with base 102 unless some internal mechanism exists to regularly clock signals through without using too much power. It is possible to include a second crystal oscillator for the

purpose of providing a lower clock frequency however this additional hardware will increase the cost and complexity of the receiver unit. The instant invention proposes a method of reducing the power consumed through the base band chip during the idle locked mode. The master clock of the baseband chip is dynamically and synchronously switched to a lower clock frequency such that less power is consumed. The present invention is easily retrofitable to current receivers without substantially altering the hardware and cost of the receiver.

Referring to FIG. 2, an example timing diagram 200 of a communications system is shown with a signal 202 that represents the DECT reference timing from base unit 102. The symbol SYNCH represents the signal that is sent every frame to receiver 104 in the DECT format to ensure that the clock timing of the receiver is aligned with the master clock reference timing of the base unit. When no communication is ongoing between the receiver and the base unit, the receiver is synchronized on every "X" DECT frame on the base unit 102 but not on every frame. Note the "X" frame in the master clock signal 204 as well. This is the time that the receiver activity 206 is starting into a suspend mode, shown by Suspend Mode signal 208, and the clock frequency does not need to remain in the higher frequency of the active mode. Each frame is 10 milliseconds in duration and the type of duty cycle dictates the number of DECT frames that the receiver circuitry tracks. During the Normal Duty Cycle (normal power consumption) "X" is equivalent to 16 DECT frames or 1 MultiFrame (or 160 ms). During thc Low Duty Cycle, "X" is equivalent to 64 DECT frames or 4 MultiFrames (or 640 ms). Therefore, synchronization will occur more frcquently when the receiver is in the Normal Duty versus the Low Duty Cycle. When the suspend mode signal 208 goes low, it is reflected by a changed master clock frequency of MCLK/N; N being a whole number divisor that decreases the mastcr clock frequency.

Referring now to FIG. 3, a timing diagram 300 resulting from an example embodiment of the present invention illustrates levels of power consumption during the idle locked mode. Specifically, base signal frames 302 define an idle state period 303 composed of a predetermined number of frames in a suspend mode 306. At the start of the idle state period the receiver 304 is synchronized with base signal 302 and

is again synchronized at the start of the next MultiFrame cycle (1 or 4, depending on the type of duty cycle). Suspend mode 306 includes active state frames and inactive state frames of the suspend mode that correspond to the master clock signal 308 and to power consumption levels 310. The active state and nominal power consumption correspond to the normal master clock frequency MCLK. The inactive state and low power consumption correspond to the master clock frequency MCLK/N, a master clock frequency that has been lowered by a divisor of N.

Referring to FIGs. 4 and 5, the schematics of the master clock signal generator coupled to the global logic of the receiver 400 and to the expanded global logic 500 illustrate an example embodiment of the present invention. In particular, master clock generator 402, that includes an oscillator circuit or a crystal oscillator, has its signal feed through a divisor 404 where it is divided by N before going into the global logic 406 of the receiver. When the baseband chip is in suspend mode or the inactive state 408, N is a whole number greater than one and divisor 404 acts to lower the master clock frequency. When the chip is in the active state and needs to resynchronize with the base unit, N equals one and the master clock frequency basically remains the same.

In FIG. 5, schematic 500 of the master clock signal generator illustrates an oscillator circuit 502 generating a 13.824 MHz signal that is clocked through a divisor 504 that has its output multiplexed through MUX 506 and into the remaining receiver logic 508. A suspend signal 510 is fed back through MUX 506 to initiate the dividing function of the master clock frequency when the suspend mode is triggered.

Referring now to FIG. 6, a timing diagram 600 illustrates an example of the suspend signal switching off the power to the receiver, made in accordance with an example embodiment of the present invention. In this example, the base unit generates a signal 602 that has a normal master clock frequency and generates a standard timing sequence. The frame boundaries are regular and are the reference points in the system. Parameters controlled in the system include:

TXFRAME register	= DECT Frame counter
MFH MFM MFL register	= DECT Multi Frame counter
SUSPFC register	= Number of DECT frames in SUSPEND mode

SUSPRFCNTL register	= Number of DECT Frames where SUSPEND (N) signal is HIGH during the active frames. (Minimum value = 2; Register = x00 & x01give also 2 frames). This register does not influence the number of suspend frames.

The suspend signal is initially designed to switch OFF the external radio module within the receiver during the suspend mode to decrease power consumption. The external radio module converts the RF signal to digital form within the receiver before being processed. When the receiver is switched ON again, the receiver needs a certain amount of time to power up and resynchronize with the base unit signal. The suspend signal approach can adjust the time period after the receiver is switched ON.

In FIG. 6, the Frame and MultiFrame counters within the base unit and the receiver are incremented automatically by the hardware of the base unit 102 and by a combination of hardware and software in receiver 104. The activity of the receiver is represented by signal 604 that synchronizes with the base once every 64 frames. The moment that the suspend signal goes high (or ends) triggers an interrupt to the microprocessor to drive an update of the Frame and MultiFrame counters within receiver 104. This occurs in the DECT timing format since the Frame and MultiFrame counters may be out of sync with the corresponding counters of the base unit. The time that suspend signal 606 is HIGH is adjustable and the signal is high when the chip is active and needs to recover the synchronization. The suspend signal is LOW when the chip is in SUSPEND mode and the master clock 610 reflects a lower signal; the lower signal having been divided by 30 in this example. DECT Frame 608 for the receiver has a number of frames defined for the suspend mode parameter SUSPFC, which is about 30 frame increments when the divisor is 30. At the sixtieth frame, suspend 606 transitions from LOW to HIGH again for four frames as the receiver is prepared for resynchronization. The master clock frequency also increases at this point to its normal rate. This LOW to HIGH transition activates the external Interrupt (ITI) to update the Frame and MultiFrame counters (through the software). The update occurs on the front edge of the SUSPEND signal when the chip goes out of the suspend mode, to ensure that the receiver is in line with the base unit

in terms of the Frame and MultiFrame numbers. Due to the fact that the master clock frequency is reduced by the divisor, the receiver Frame and MultiFrame counters may not have the same value as the base unit counter.

Working through the specific example as simply an illustration, the parameter values depend on MCLK division as shown in the table below (based on Low duty cycle mode):

MCLK / N	SUSPFC	SUSPRFCNTL	TXFRAME	Multi Frame counter
CLK = MCLK	63	2	No adjustment	No adjustment
CLK = MCLK / 30	5	4	13	+ 3

Table 6-1: Parameters

In order to calculate SUSPFC, the following formulas are used :

NbFSM = (SUSPFC – SUSPadd) * N + SUSPadd

SUSPFC = SUSPadd + (NbFSM - SUSPadd) / N

Where:

NbFSM = Number of Frame in suspend mode
In the LOW Duty cycle mode => NbFSM = 63.

In Normal Duty cycle mode => NbFSM = 15.
SUSPadd = SUSPRFCNTL – 1
Because of SUSPRFCNTL, it is possible to find an integer in the formula.
SUSPadd = 4 – 1 = 3
SUSPFC = 3 + (63 – 3)/15 = 7

TXFRAME value depends on SUSPRFCNTL and can be easily found since the synchronization always occurs on Slot 0.

The Multi Frame Counter correction (MFCC) can be calculated as follows:

MFCC = 3 – SUSPFC/16; where MFCC is an integer.

This formula is effective as long as SUSPRFCNTL < 16.

The following illustrates the resulting power consumption during normal master clock signaling conditions:

CLK = MCLK	After Reset	LOCK+SUSPEND
Power (mW)	6.48	8.43

When the divisor is incorporated into the circuit, the following occurs:

CLK = MCLK / 30	After Reset	LOCK+SUSPEND
Power (mW)	6.56	0.35

Note that in this example a power consumption reduction of about 20 times was achieved using an embodiment of the present invention. One of thc advantages to this approach is that the logic required to implement this method does not overly complicate an existing hardware design and can partly be achieved through software modifications.

Referring to FIG. 7, a schematic diagram 700 of the global logic implementing the example embodiment described in FIG. 6 illustrates the example logic readily implemented to realize the example embodiment of the present invention. Master clock 702 serves as an input signal to counter 704, while a suspend mode signal 704 is an input to a flip-flop 708 and to a NOR gate 710. The output of counter 704 is combined at NOR gate 710 and another output is passed through an inverter 712 before serving as an input to a MUX 714. The output of NOR gate 710 is feedback into counter 704, thereby affecting the master clock signal going into MUX 714. The output of MUX 714 is the clock output that is feed to the global logic of the receiver. The output of MUX 714 reflects the changed clock frequency depending on the divisor.

The various cmbodiments described above are provided by way of illustration only and are not intended to limit the invention. Those skilled in the art will readily

recognize various modifications and changes that may be made to the present invention without strictly following the examplc embodiments and applications illustrated and described herein. The scope of the present invention is set forth in the following claims.

What is claimed is:

A method of reducing power consumption of a receiver of a communications device, the receiver having an internal power source and a corresponding base unit, the receiver adapted to receive a transmitted signal in the form of a data stream, the stream defined by a plurality of frames, each of the frames including a synchronization sub-frame, the method comprising the steps of:

detecting the activity status of the receiver with respect to the transmitted signal, the receiver being in an idle state when not receiving a transmitted signal, the idle state defined by a predetermined number of frames that include a set of active state frames and inactive state frames that combine to define a duration of the idle state;

generating a clock signal that has an output frequency that varies as a function of the active and inactive frames, the clock frequency being higher in the active state and lower in the inactive state, such that the receiver consumes more power during the active state than when in the inactive state;

synchronizing the receiver with the sub-frame of the transmitted signal during the idle state; and

reducing power consumption of the receiver by reducing the clock frequency as the number of inactive frames within the idle state are increased, power consumption being a function of the power consumed during the active and inactive states and the duration of the idle state.

2. The method of claim 1, wherein the step of reducing power consumption includes decreasing the number of active frames.

3. The method of claim 1, wherein the idle period length remains unchanged irrespective of the clock frequency output.

4. The method of claim 1, wherein the frames of the idle state have a frame boundary with a programmable length.

5. The method of claim 4, wherein the active and inactive frames start and stop on the frame boundary.

6. The method of claim 1, wherein the clock frequency is decreased during the inactive state by a factor of N, where N is a number greater than 1.

7. The method of claim 1, further including the step of synchronizing a frame counter of the receiver with a frame counter of the base unit at the end of the active state.

8. The method of claim 7, further including the step of synchronizing a multiframe counter of the receiver with a multiframe counter of the base unit at the end of the inactive state.

9. The method of claim 1, wherein reducing power consumption of the receiver includes dynamically and synchronously switching to a low clock frequency corresponding to the inactive state as the number of inactive frames within the idle state are increased.

10. The method of claim 9, further including the step of synchronizing a multiframe counter of the receiver with a multiframe counter of the base unit at the end of the inactive state.

FIG. 1
PRIOR ART

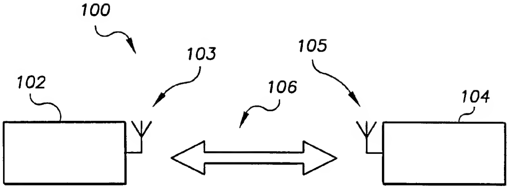


FIG. 2

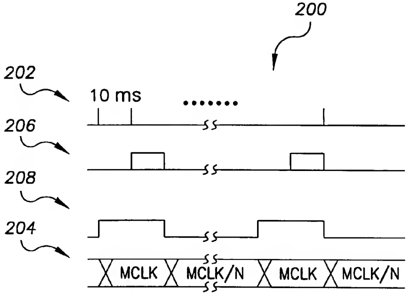


FIG.3

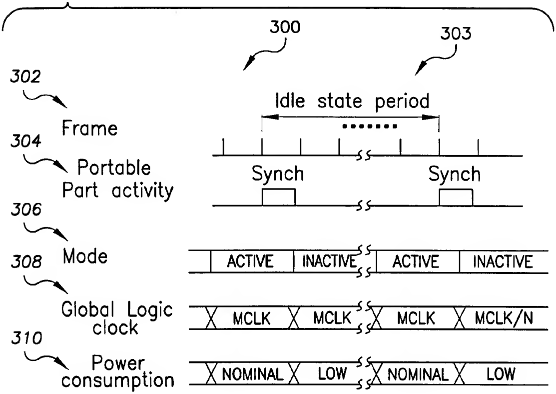
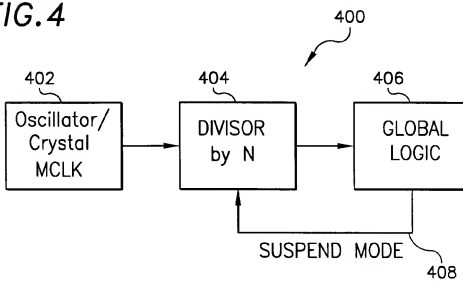

300
303
302
Idle state period
Frame
304
Portable Part activity
Synch
Synch
306
Mode
ACTIVE
INACTIVE
ACTIVE
INACTIVE
308
Global Logic clock
MCLK
MCLK
MCLK
MCLK/N
310
Power consumption
NOMINAL
LOW
NOMINAL
LOW

FIG.4


400
402
Oscillator/ Crystal MCLK
404
DIVISOR by N
406
GLOBAL LOGIC
SUSPEND MODE
408

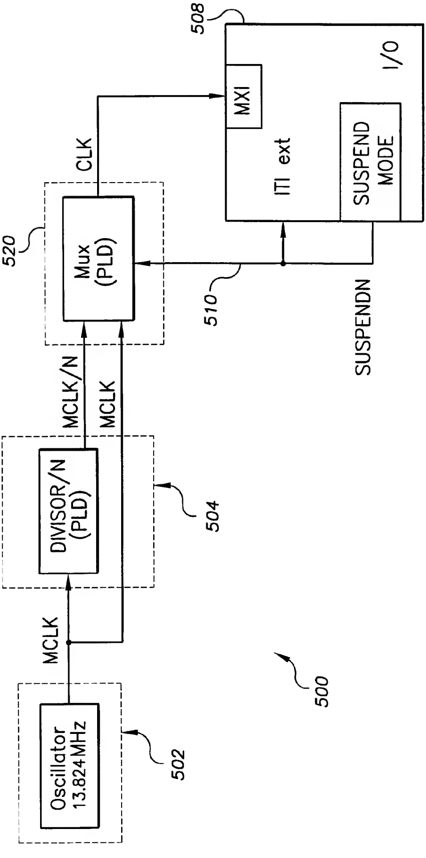

Oscillator
13.824MHz
502
MCLK
DIVISOR/N
(PLD)
504
MCLK/N
MCLK
Mux
(PLD)
520
CLK
510
SUSPENDN
508
MXI
ITI ext
SUSPEND
MODE
I/O
500

FIG.5

FIG.6

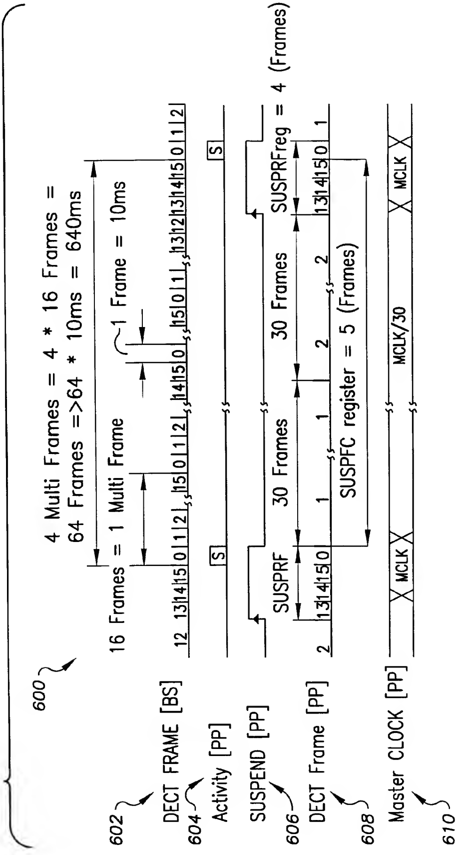

600
602
DECT FRAME [BS]
604
Activity [PP]
SUSPEND [PP]
606
DECT Frame [PP]
608
Master CLOCK [PP]
610
4 Multi Frames = 4 * 16 Frames =
64 Frames =>64 * 10ms = 640ms
16 Frames = 1 Multi Frame
1 Frame = 10ms
12 13 14 15 0 1 2 15 0 1 2 14 15 0 15 0 1 13 12 13 14 15 0 1 2
S
S
SUSPRF
30 Frames
30 Frames
SUSPRFreg = 4 (Frames)
2 13 14 15 0 1 1 2 2 13 14 15 0 1
SUSPFC register = 5 (Frames)
MCLK
MCLK/30
MCLK

FIG.7-1

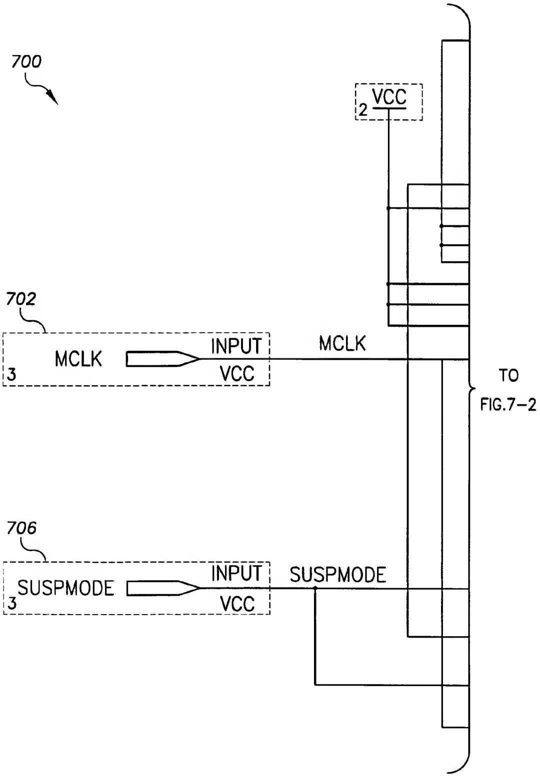

700
2 VCC
702
MCLK
INPUT
VCC
3
MCLK
TO
FIG.7-2
706
SUSPMODE
INPUT
VCC
3
SUSPMODE

FIG.7-2

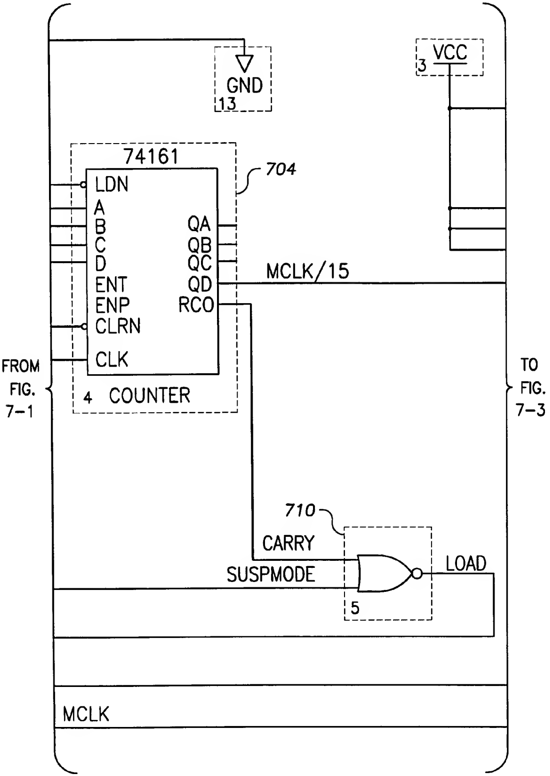

GND
13
VCC
3
74161
704
LDN
A
B
C
D
ENT
ENP
CLRN
CLK
QA
QB
QC
QD
RCO
MCLK/15
4 COUNTER
FROM FIG. 7-1
TO FIG. 7-3
710
CARRY
SUSPMODE
LOAD
5
MCLK

FIG. 7-3

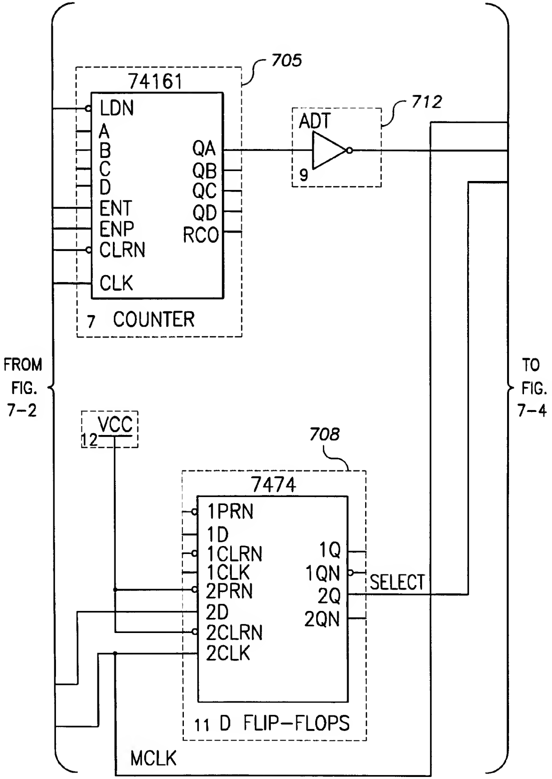
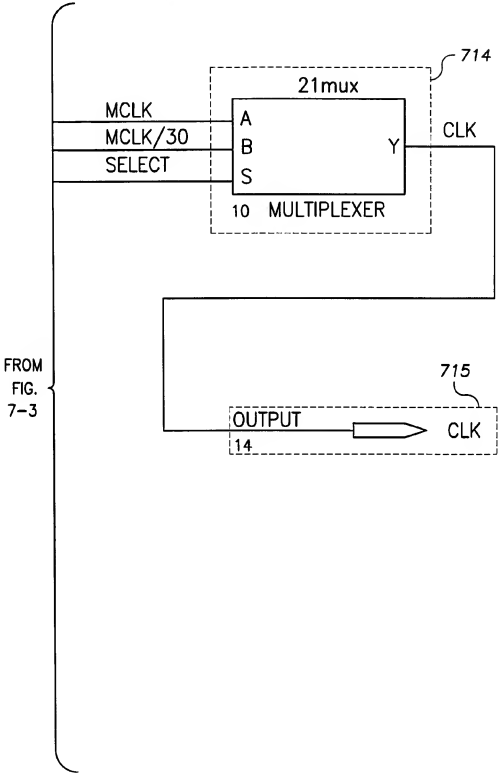

705
74161
LDN
A
B
C
D
ENT
ENP
CLRN
CLK
QA
QB
QC
QD
RCO
7 COUNTER
712
ADT
9
FROM
FIG.
7-2
TO
FIG.
7-4
VCC
12
708
7474
1PRN
1D
1CLRN
1CLK
2PRN
2D
2CLRN
2CLK
1Q
1QN
2Q
2QN
SELECT
11 D FLIP-FLOPS
MCLK

FIG.7-4


714
21mux
MCLK
MCLK/30
SELECT
A
B
S
Y
CLK
10 MULTIPLEXER
FROM FIG. 7-3
715
OUTPUT
14
CLK